

REMARKS

Claims 1-20 are now present in this application.

The title and claims 1, 2 and 9 have been amended and claims 16-20 have been presented. Reconsideration of the application, as amended, is respectfully requested.

The Examiner has objected to the title. Since this Examiner's proposal has been followed, it is submitted that any objection to the title should now be overcome and withdrawn.

Claim 9 is objected to because of an informality. Because this informality has been corrected, this objection should now be reconsidered and withdrawn.

Claims 1-15 stand rejected under 35 USC 112, first paragraph. This rejection is respectfully traversed.

Claims 1, 2 and 9 have now been modified based on paragraphs [0012], [0021], [0022] and [0005]. In particular, paragraph [0012] states, "That is, after a data transmission signal (hereinafter, referred as to LOAD) is triggered and before a data reception signal (hereinafter, referred as to DSTH) is triggered...". It is obvious that the data transmission signal is referred to as the LOAD signal, and the data reception signal is referred to as the DSTH signal. The LOAD signal and the DSTH signal are defined in detail in the paragraph [0022]. Paragraph [0022] describes, "The DSTH signal controls the data input to the timing controller. The LOAD signal controls the data input to the display panel." In addition, paragraph [0021] recited "A driver circuit of a liquid crystal display device according to the invention includes a timing controller and a source driver. The timing controller receives an image data and outputs a digital image signal. The source driver receives the digital image signal and generates an analog image signal." The source driver is defined in paragraph [0005] in that "FIG. 1 ...The source driver 120 receives TTL data 302 from the timing controller 110 and accordingly generates an analog signal 303 for controlling a liquid crystal display panel 200." Therefore, it is obvious that the timing controller is driven by the DSTH signal based on the combination of the paragraph [0022]

and [0021]. The source driver is driven by the LOAD signal to generate the analog signal for controlling the liquid crystal display panel.

It is respectfully submitted that an enabling disclosure is provided and the claims should not be rejected under 35 USC 112, second paragraph. As such, it is requested that this rejection now be reconsidered and withdrawn.

Claims 1-3, 5-6, 8-10, 12-13 and 13 stand rejected under 35 USC 103 as being unpatentable over the Admitted Prior Art in view of US Patent 6,414,670 to Kim. This rejection is respectfully traversed.

Claims 4, 7, 11 and 14 stand rejected under 35 USC 103 as being unpatentable over the Admitted Prior Art in view of the patent to Kim and further in view of US Patent 5,615,376 to Ranganathan. This rejection is respectfully traversed.

In the invention, a timing controller receives an image data and outputs a digital image signal. A data reception signal (DSTH signal) determines the programming time of the timing controller receiving the image data. The DSTH signal controls the image data input to the timing controller. A clock signal (DCLK signal) is applied for the timing controller. The timing controller is operated in the DCLK signal and is driven by the DSTH signal to receive the image data. The timing controller outputs a data transmission signal (LOAD signal) and a digital image signal according to the image data. The source driver receives the LOAD signal and digital image signal, and generates an analog image signal. The LOAD signal confirms the programming time of the data into the display panel. The LOAD signal controls the source driver to receive the digital image signal from the timing controller, and drives the source driver to output the analog image signal input to the display panel. While the LOAD signal is switched on and the DSTH signal is not switched on, the timing controller is not energized to receive the image data. At this time, the DCLK signal is still transmitted and applied for the timing controller, which wastes the electrical current.

The Kim reference (6,414,670) provides a gate driving circuit that includes a plurality of clock control circuits and gate drivers. Each gate driver receives a pulse input signal STV1, and shifts the pulse input signal STV1 to output a pulse output signal STV2. The pulse output signal STV2 is shifted from the pulse input signal STV1. The pulse output signal STV2 from the former gate driver is the pulse input signal STV1 of the next gate driver. The pulse input signal STV1 and the pulse output signal STV2 are applied for driving the gate driver. Each clock control circuit control a clock signal, which is applied for the corresponding gate driver, in response to the pulse input signal STV1 and the pulse output signal STV2. Thus, the corresponding gate driver is entire no work resulting from the disable clock signal.

However, the invention is applied in a timing controller not a gate driving circuit. In the timing controller, a circuit for receiving the image data is not work resulting from the disable clock signal (DCLK), but other circuit for outputting the digital image signal is still working. The Kim reference and the invention therefore have different applications and results.

The APA discloses a DSTH signal and a LOAD signal. However, the DSTH signal and the LOAD signal are not shifted from each other. Both the DSTH signal and the LOAD signal are not applied for driving the gate driver. The DSTH signal controls the image data input to the timing controller, and the LOAD signal controls the source driver. The pulse input signal STV1 and the pulse output signal STV2 in the Kim reference are quite different from the DSTH signal and the LOAD signal. One of ordinary skill in the art would not try to modify the Admitted Prior Art with the teachings of the Kim reference.

The combination of the Kim reference and the APA is improper because the Kim reference and the APA have different ways of implementation, and one skilled in the art would have no reason to make such a combination. Because of the above, claim 1-3, 5-6, 8-10, 12-13 and 15 would be allowable. The 35 USC 103 rejection should be withdrawn.

The secondary reference to Ranganathan discloses a clock management that operates for a CRT scan. The Ranganathan reference, however, does not disclose how to work in an LCD

with circuits ex: timing controller, gate driver, or source driver. However, the invention operates when the timing controller does not receive image data but outputs the digital image signal. The Ranganathan reference and the invention have different applications and results.

The combination of the Kim reference, the Ranganathan reference and the APA is submitted to be improper because the Kim reference and the Ranganathan reference have different applications and results, and one skilled in the art would have no reason to make such a combination. The teachings of Ranganathan also do not overcome the problems with the APA and Kim combination as noted above. Because of this, claim 4, 7, 11, 14 are also allowable. The rejection using the Ranganathan reference should also be reconsidered and withdrawn.

Withdrawal of all objections and rejections and allowance of the instant application are earnestly solicited.

Because the additional documents cited by the Examiner have been included merely to show the state of the prior art and have not been utilized to reject the claims, no further comments concerning these documents should be necessary at this time.

The Examiner is invited to contact the undersigned at 703-205-8000 in the Washington, D.C. area if any matters remain outstanding in this application.

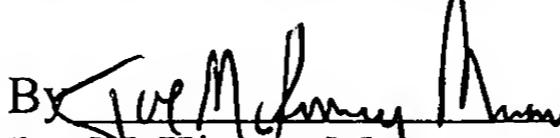
Pursuant to 37 C.F.R. §§ 1.17 and 1.136(a), Applicant respectfully petitions for a two (2) month extension of time for filing a reply in connection with the present application, and the required fee of \$450.00 is attached hereto.

In view of the above amendment, applicant believes the pending application is in condition for allowance.

If necessary, the Commissioner is hereby authorized in this, concurrent, and future replies, to charge payment or credit any overpayment to Deposit Account No. 02-2448 for any additional fees required under 37 C.F.R. §§ 1.16 or 1.17; particularly, extension of time fees.

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Respectfully submitted,

By 
Joe McKinney Muncy
Registration No.: 32,334
BIRCH, STEWART, KOLASCH & BIRCH, LLP
8110 Gatehouse Road
Suite 100 East
P.O. Box 747
Falls Church, Virginia 22040-0747
(703) 205-8000
Attorney for Applicant